

# Improved SiC Power MOSFET Model Considering Nonlinear Junction Capacitances

Zhuolin Duan , Tao Fan, *Member, IEEE*, Xuhui Wen, *Senior Member, IEEE*, and Dong Zhang

**Abstract**—Silicon carbide (SiC) power metal–oxide–semiconductor field-effect transistors (MOSFETs) have been applied in high-power and high-frequency converters recently. To effectively predict characteristics of SiC power MOSFETs in the design phase, a simple and valid model is needed. In this paper, a simple improved SiC power MOSFET behavioral model is proposed using SPICE language. Key parameters in the model are analyzed and determined in detail, including parasitic parameters of the power module, steady-state characteristic parameters, and nonlinear parasitic capacitances. The effect of negative turn-OFF gate drive voltage is considered and a continuously differentiable function is proposed to describe the gate–source capacitance. Experimental validation is performed under a double pulse circuit employing an *N*-channel power MOSFET half-bridge module CAS300M12BM2 (Cree Inc.) rated at 300 A/1200 V. The main switching dynamic characteristic parameters of the model have been compared with those of the measured results. The results show that taking gate–source capacitance as a linear value as most previous models do will cause significant turn-ON deviations between experiment and simulation results, while the improved model is more accurate compared with the measured results.

**Index Terms**—Behavioral model, metal–oxide–semiconductor field-effect transistors (MOSFETs), silicon carbide (SiC).

## I. INTRODUCTION

IN THE past few decades, with the great development of wide-bandgap semiconductor materials, especially silicon carbide (SiC), considerable progress of power semiconductor devices based on SiC has been made in many applications [1].

Since metal–oxide–semiconductor field-effect transistor (MOSFET) is a widely-used transistor in industrial applications, such as motor drive systems, a lot of attention has been drawn to SiC power MOSFET. Compared with Si MOSFET, SiC power MOSFET has a lot of superior characteristics, such as smaller ON-state resistance, higher switching speed, higher switching frequency, and higher operating temperature [2], [3]. Hence, it

is quite applicable for industrial power products which require high temperature, high frequency, or high-power density, and it has gradually been popular in many applications.

In order to evaluate the characteristics of SiC power MOSFET such as electromagnetic interference (EMI) characteristics and power losses, and to evaluate the converter functions in design phase, an accurate model is needed, which should not be too complex as well [4]–[6].

So far, there have been many SiC MOSFET modeling methods in previous reports. In [7], a review of SiC MOSFET models presented in the literature is presented. The physical numerical models in [8] and [9], which are based on the carrier drift–diffusion motion equations, are always too complex to be implemented in circuit simulations. Thus, behavioral models should be adopted in circuit simulations. Some types of simulation software, such as Saber and PSpice, provide built-in MOSFET models [10]–[12]. But often they can only be used in one specific simulator and cannot be easily transplanted to other types of software. At the same time, the accuracy of these models is often not enough for switching transient processes. Due to the fast switching speed of SiC MOSFET, parasitic capacitances should be well modeled. In [13], a simple SPICE behavioral model of a 5 A/10 kV SiC MOSFET is given, which is based on specific modification on the conventional level-1 commercial SPICE MOSFET model. A modified switch model for the nonlinear gate–drain capacitance  $C_{gd}$  is presented. But a lot of efforts are needed to extract factors from measured curves to obtain accurate  $C_{gd}$  model. For the gate–source capacitance  $C_{gs}$ , in most previous models, it is treated as a constant.

In this paper, a low-complexity and improved behavioral modeling method is proposed. Module parasitic parameters, steady-state characteristics, and interelectrode capacitances are modeled. Since the device datasheet does not provide enough information for building an accurate model, some parameters of interelectrode capacitances are determined by measurement. The effect of negative gate drive voltage is considered and  $C_{gs}$  is redefined. A hyperbolic-tangent-based function is proposed to describe  $C_{gs}$ , thus convergence problems can be avoided. Compared with previous models which take  $C_{gs}$  as a linear value, the model can avoid deviations between experiment and simulation turn-ON transient waveforms and is more accurate. In addition, the model is simple enough and very suitable to be used in circuit simulations. A SiC power MOSFET half-bridge module, named CAS300M12BM2 [14] released by Cree Inc., rated at 300 A/1200 V, has been employed for experimental tests. Finally, the performance of the model has been verified

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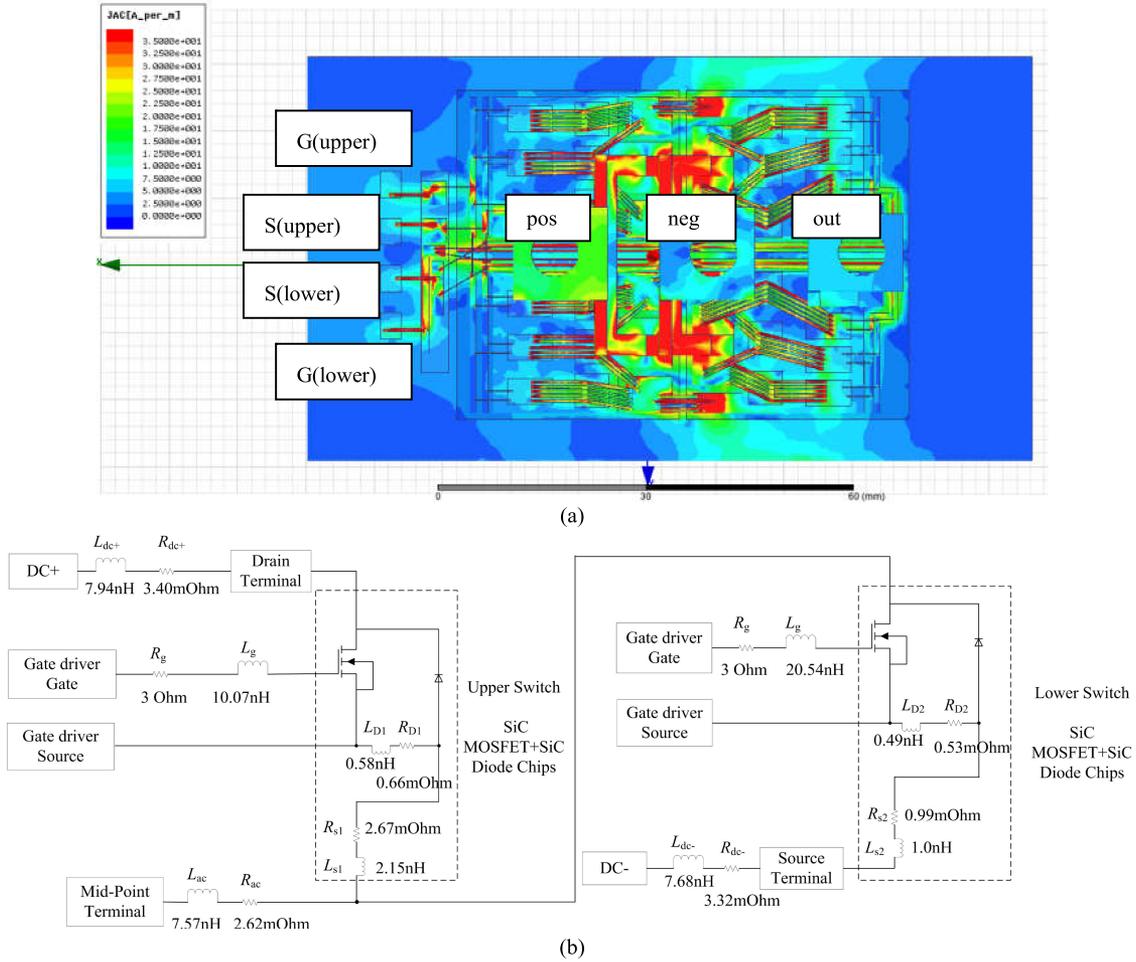


Fig. 1. CAS300M12BM2 module. (a) Current density distribution in ANSYS Q3D. (b) Schematic of the electrical circuit including parasitic inductances and resistances.

through a double pulse test circuit by comparisons between simulation and experiment results. In addition, temperature characteristics of the model are not concerned in this paper, so the modeling method does not take temperature characteristics into consideration.

## II. BEHAVIORAL MODELING FOR THE SiC POWER MOSFET

The investigated SiC power MOSFET is a half-bridge module encapsulated in a standard 62-mm package. Stray parameters of the power module, such as  $L_d$ ,  $L_s$ ,  $L_g$ , strongly influence switching performances of the MOSFETs and may induce resonance, thus need to be considered in the device modeling procedure. By the software ANSYS Q3D, extraction of parasitic parameters of the power module has been realized. The extracted parasitic elements results are inductance and resistance matrices at a given frequency. The current density distribution of the module in Q3D and its electrical circuit schematic with extraction results are shown in Fig. 1.

As shown in Fig. 1(a), most of the current is concentrated toward terminal pins. Thus, stray inductances of terminal pins have great influence on switching performances.

Behavioral model of the basic power MOSFET chip can be drawn as Fig. 2.

As shown in Fig. 2,  $M_1$  and  $D_{\text{body}}$  are used to describe the basic characteristics of  $N$  channel MOSFET. Interelectrode capacitances  $C_{gs}$ ,  $C_{gd}$ , and  $C_{ds}$  are used to reflect the dynamic characteristics. The drain-source capacitance  $C_{ds}$  is a PN junction capacitance between drain and source, which does not appear in Fig. 2 because it can be realized by junction capacitance of the diode. The antiparalleled diode is modeled using the diode model provided by LTspice. The required parameters in the diode model, such as saturation current  $I_s$ , emission coefficient  $n$ , capacitance gradient factor  $m$ , junction potential  $v_j$ , ohmic resistance  $r_s$ , forward transit time  $tt$ , can be extracted by manufacturer datasheet.  $R_g$  is the internal gate resistance, which can be measured by an LCR meter.

Then, the modeling method using SPICE language will be expounded in detail, mainly including the modeling methods of steady-state characteristics and interelectrode capacitances.

### A. Steady-State Characteristics Modeling of SiC MOSFET

To describe the steady-state characteristics of MOSFET, the Shichman-Hodges model [15] is adopted, for it is simple and

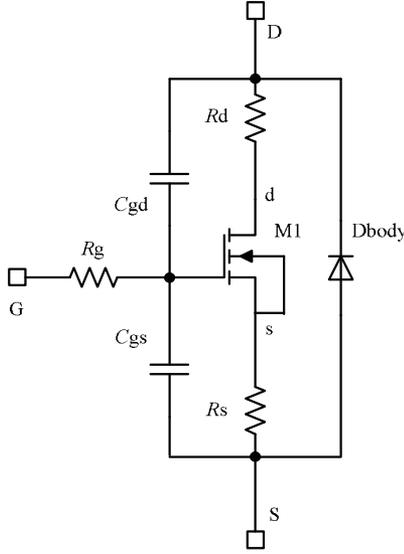


Fig. 2. Behavioral model of power MOSFET chip.

its simulation time is short. When the gate to source voltage  $V_{gs}$  is lower than the threshold voltage  $V_{th}$ , the MOSFET turns OFF and the drain current  $I_d$  is set as zero. When  $V_{gs}$  is higher than  $V_{th}$ , MOSFET works normally, and the working region can be divided into two cases. If the “internal” drain to source voltage  $V_{ds}$  is larger than  $(V_{gs} - V_{th})$ , the MOSFET works in the saturation region, else it works in the linear region. In the saturation region, the drain current can be written as

$$I_d = 0.5 K_P (1 + \lambda V_{ds}) (V_{gs} - I_d R_s - V_{th})^2 \quad (1)$$

where  $V_{th}$  represents the threshold voltage,  $K_p$  is a parameter of the transconductance,  $\lambda$  is the coefficient of channel length modulation, and  $R_d, R_s$  are drain and source resistances, respectively. Compared with the long channel,  $\lambda$ , which represents the relative variation of channel length, is very small and can be treated as zero. Then, by choosing points from the saturation region of device output characteristic curves in the datasheet, basic parameters  $V_{th}, K_p$ , and  $R_s$  can be extracted by (1).

In the linear region, the drain current can be written as

$$I_d = K_P (1 + \lambda V_{ds}) (V_{gs} - V_{th} - I_d R_s - 0.5 V_{ds}) V_{ds}. \quad (2)$$

The ON-state resistance  $R_{ds(on)}$  is a reciprocal of the slope of output characteristic curve in linear region. To calculate  $R_{ds(on)}$ , (2) needs to be simplified. Also,  $\lambda$  is treated as zero. Because in linear region  $0.5 V_{ds}$  is relatively small compared with  $(V_{gs} - V_{th})$ , thus it is ignored. By applying a 1 V voltage between the external drain and source, it can be derived that  $I_d = 1/R_{ds(on)}$ , and  $V_{ds} = 1 - (R_d + R_s)/R_{ds(on)}$ . Then, the following equation can be derived from (2):

$$R_{ds(on)} = R_d + R_s + 1 / (K_p (V_{gs} - V_{th} - R_s / R_{ds(on)})). \quad (3)$$

By (3),  $R_d$  can be calculated by choosing points from the linear region of device output characteristic curves in the datasheet. The internal gate resistance  $R_g$  can be measured by an LCR meter.

After modeling steady-state characteristics, the transfer characteristic curve and output characteristic curves can be achieved.

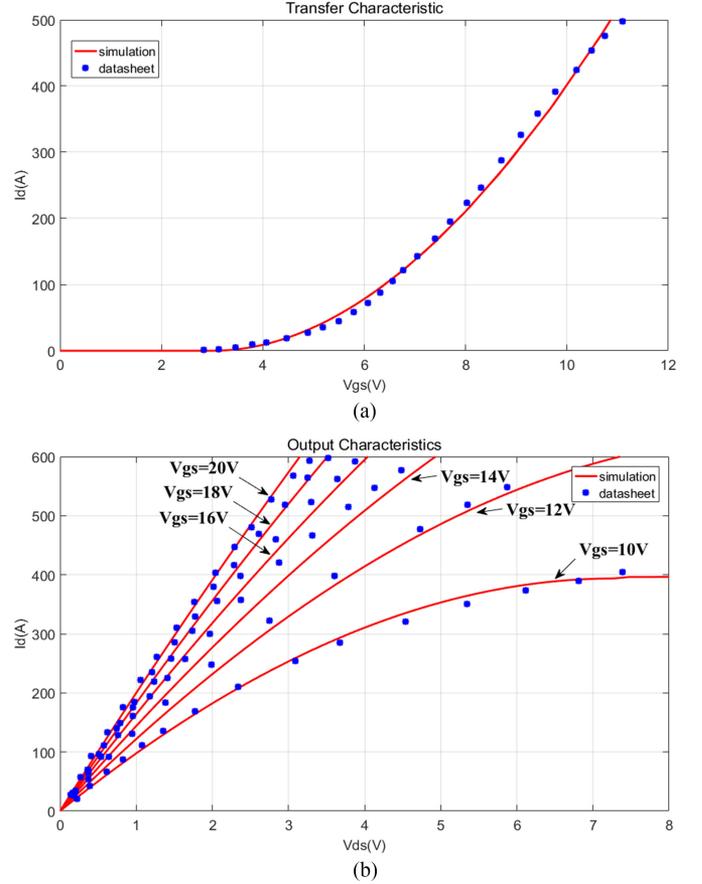


Fig. 3. Steady-state characteristic curves comparison. (a) Transfer characteristic. (b) Output characteristics.

Then, the simulated curves are compared with the datasheet curves, and the results are shown in Fig. 3.

As shown in Fig. 3, with the simple modeling and parameter extraction method, a satisfied accuracy of the simulated steady-state characteristics compared with datasheet values has been achieved.

### B. Modeling of Interelectrode Capacitances

The three nonlinear interelectrode capacitances  $C_{gs}, C_{gd}$ , and  $C_{ds}$  considerably impact transient switching processes. Therefore, to establish precise high-frequency power MOSFET model, correct description of these capacitance characteristics is needed.

For SiC power MOSFET, considering reliable turn-OFF,  $-5$  to  $-2$  V negative turn-OFF gate drive voltage is often employed. When the gate voltage crosses zero and becomes negative, the gate–source capacitance increases and reaches the value of the oxide capacitance [16]. Thus,  $C_{gs}$  is treated as a linear value, as most previous models may lead to inaccuracy between experiment and simulation results. In [17], an optional capacitance in series with a switch is added in parallel with the original linear value to describe  $C_{gs}$  when the gate voltage is negative. But this discontinuous behavior of  $C_{gs}$  may create convergence problems, thus the method is not suitable for circuit simulations. For numerical modeling of a nonlinear capacitance, the expression used should have continuous derivative in the used range,

and a possibility of independent selection of minimum and maximum values. When  $V_{gs}$  is positive,  $C_{gs}$  reaches the minimum value and when  $V_{gs}$  is negative,  $C_{gs}$  reaches the maximum value. Thus, it is proposed to use a hyperbolic-tangent-based function to describe  $C_{gs}$  as follows:

$$C_{gs} = 0.5 C_{gsmin} (1 - \tanh(v(g, s))) + C_{gsmin} \quad (4)$$

where  $C_{gsmin}$  is the gate–source capacitance when the gate drive voltage is positive and  $C_{gsmax}$  is the gate–source capacitance increment when the gate voltage is negative, which can be adjusted by experiment results or experience. By this expression, the value of  $C_{gs}$  can be more exactly described and it is simple and suitable to be used in simulations.

For SiC power MOSFET, capacitance  $C_{gd}$  varies dramatically with  $V_{gd}$ . When  $V_{gd}$  is negative,  $C_{gd}$  is physically the series connection of the gate oxide capacitance  $C_{ox}$ , with the depletion layer capacitance under gate oxide. This capacitance is fairly low due to the thickness of the nonconducting die, it is the minimum value of  $C_{gd}$  and is defined as  $C_{gdmin}$ . When  $V_{gd}$  is positive, the die is conducting and  $C_{gd}$  is physically  $C_{ox}$ , it is the maximum value of  $C_{gd}$  and is defined as  $C_{gdmax}$ . Since it is hard to read  $C_{gdmin}$  and  $C_{gdmax}$  values from the datasheet graph, an experimental method proposed in [18] is used to obtain the values. The method extracts the capacitances by switching waveforms measured during a turn-ON process in the half-bridge test circuit.

The following empirical formula is used to describe the non-linear parasitic capacitance  $C_{gd}$  [19]:

$$C_{gd} = \begin{cases} A \tanh(aV_{gd}) + B, & \text{if } V_{gd} > 0 \\ C a \tanh(aV_{gd}) + D, & \text{if } V_{gd} < 0 \end{cases} \quad (5)$$

where the constant parameters  $A$ ,  $B$ ,  $C$ , and  $D$  are calculated depending on  $C_{gdmin}$  and  $C_{gdmax}$  values. Parameters  $A$  and  $C$  are the slopes of the  $\tanh$  and  $\tanh$  curves when  $V_{gd} = 0$ , respectively, and they are equal. Parameters  $B$  and  $D$  determine the crossover value when  $V_{gd} = 0$  and they are equal. Parameter  $a$  is tuned to fit the slope of  $C_{gd}$  with the datasheet graph.

Since  $C_{gd}$  is a variable capacitance, a challenge in the SPICE modeling is how to express variable capacitance equations and how to diminish the risk of convergence problems [20]. The following method is used to realize the variable capacitance. A variable capacitance model can be treated as an arbitrary voltage source by

$$V_c(t) = \frac{1}{C} \int I_c(t) dt. \quad (6)$$

By making the current of the variable capacitance go through a 1 F capacitance, the voltage on the 1 F capacitance can be read as the current integral term  $\int I_c(t) dt$ . Then, the variable capacitance model in (6) is realized as shown in Fig. 4, where  $V(ctrl)$  is the expression of  $C_{gd}$ , namely (5), and  $V(int)$  is the voltage on the 1 F capacitance.

Capacitance  $C_{ds}$  is constituted by the MOSFET drain–source capacitance paralleled with free-wheeling diode capacitance. It varies with the depletion width of PN junction, which depends on drain–source voltage  $V_{ds}$ , and it can be described by the

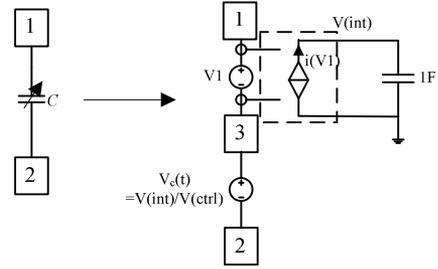


Fig. 4. Variable capacitance realization circuit.

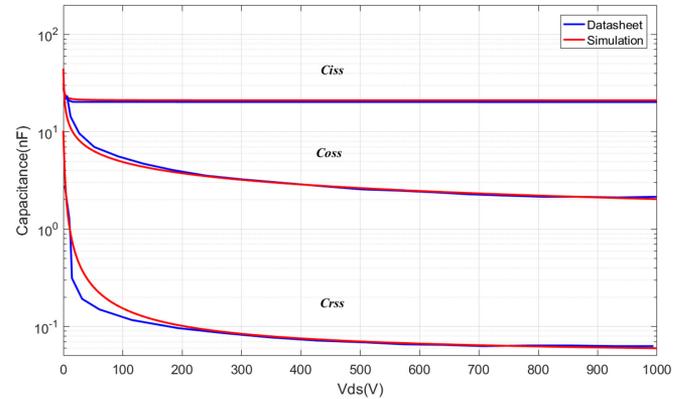


Fig. 5. Values of parasitic capacitances in relationship with the drain–source voltage.

following equation [21]:

$$C_{ds} = C_{j0} \left( 1 + \frac{V_{ds}}{V_j} \right)^{-m} \quad (7)$$

where  $C_{j0}$  is the value of  $C_{ds}$  when  $V_{ds} = 0$ , which can be derived by the output capacitance  $C_{oss}$  minus the gate–drain capacitance at  $V_{ds} = 0$ . The output capacitance at  $V_{ds} = 0$ , which is  $C_{ossmax}$ , can be identified using the manufacturer datasheet.  $V_j$  is the built-in voltage of diode and can be treated as an undetermined coefficient.  $m$  is the capacitance gradient factor. Ignoring the temperature characteristics, by fitting the slope of the output capacitance  $C_{oss}$  curve in the datasheet, these parameters can be determined.

Parasitic capacitances  $C_{iss}$ ,  $C_{rss}$ , and  $C_{oss}$  listed in the datasheet can be represented by parasitic capacitances  $C_{gs}$ ,  $C_{gd}$ , and  $C_{ds}$  as follows:

$$\begin{aligned} C_{iss} &= C_{gs} + C_{gd} \\ C_{rss} &= C_{gd} \\ C_{oss} &= C_{gd} + C_{ds}. \end{aligned} \quad (8)$$

Then, the simulated capacitance results compared with the datasheet curves are shown in Fig. 5. The blue lines are the datasheet curves, and the red lines are the simulated capacitance curves.

It can be found in Fig. 5 that, within most of the working range, the simulated capacitance curves match well with the datasheet curves.

Finally, parameters of the model are listed in Table I.

TABLE I  
BEHAVIORAL MODEL PARAMETERS

Parameter	Value	Unit	Parameter	Value	Unit
$K_p$	17.832	$A/V^2$	$C_{gsmin}$	21	nF
$V_{th}$	2.5	V	$C_{gsm}$	12	nF
$\lambda$	0.001	$V^{-1}$	$C_{gdmin}$	150	pF
$R_d$	0.0007	Ohm	$C_{gdmax}$	13 176	pF
$R_s$	0.0009	Ohm	$a$	0.6	–
$I_s$	$8.35e-4$	A	$C_{j0}$	35	nF
$N$	3.298	–	$m$	0.39	–
$V_j$	0.69	V	$r_s$	0.002	Ohm

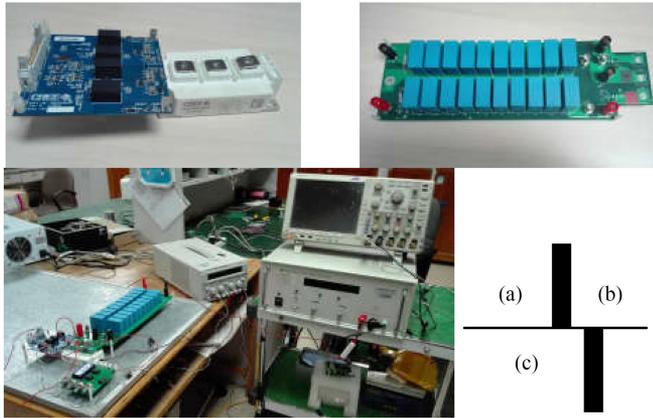


Fig. 6. Photograph of the test platform (a) SiC MOSFET module and driver. (b) The PCB with capacitors. (c) Test layout.

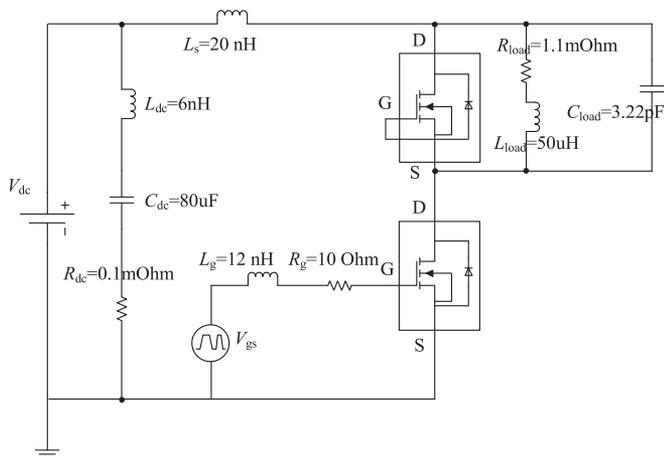


Fig. 7. Simulation circuit for switching transient test.

### III. COMPARISON BETWEEN EXPERIMENT AND SIMULATION RESULTS

To verify the analysis and modeling method in the previous section, a typical double pulse test circuit is built based on an inductive clamped circuit. Fig. 6 shows the photograph of test platform. The 1200 V 300 A SiC MOSFET half-bridge module CAS300M12BM2 from Wolfspeed corporation is tested. A gate driver CGD15HB62P-32 also from Wolfspeed corporation is used, which provides a 9 A maximum drive current, and a  $-5$  to 20 V drive voltage. A 10- $\Omega$  resistance is used as the external

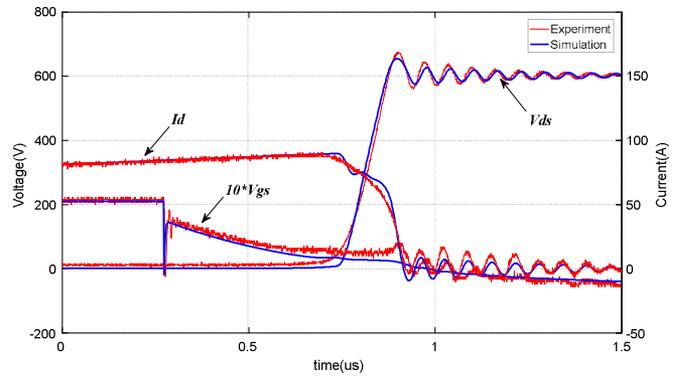


Fig. 8. Comparison of experiment and simulation turn-OFF waveforms with the improved model @600 V 85 A.

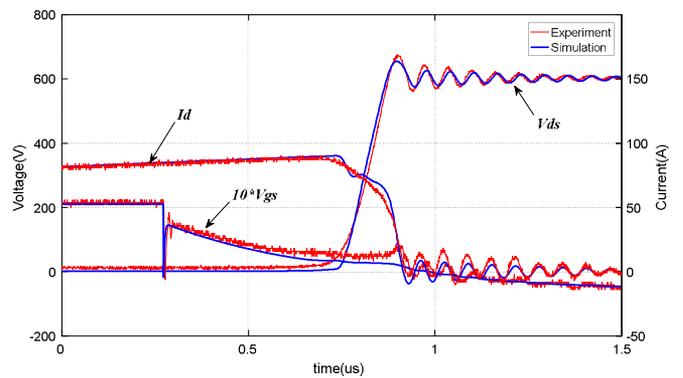


Fig. 9. Comparison of experiment and simulation turn-OFF waveforms with the model of linear  $C_{gs}$  @600 V 85 A.

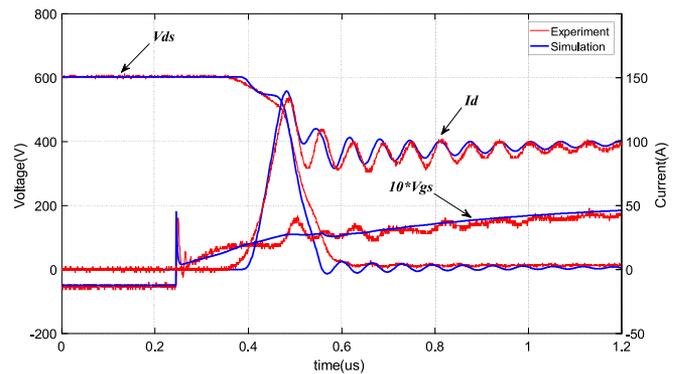


Fig. 10. Comparison of experiment and simulation turn-ON waveforms with the improved model @600 V 85 A.

gate resistance. Parasitic inductance of the gate circuit is measured by an Agilent E4990A impedance analyzer, which is about 12 nH. A 50  $\mu$ H ferrite-core inductor is used as the load inductor. A printed circuit board (PCB) with 80  $\mu$ F input polypropylene capacitance, which was designed to minimize the parasitic inductances, was built to conduct the experiment. The test circuit was fed by 600 V dc supply voltage. Switching voltage measurements were carried out with the Tektronix DPO4054B, 500-MHz oscilloscope, equipped with voltage probes: GTP-100A-4 (600 V/100 MHz). Switching current was measured by an ultramini Rogowsky Current Transducer: CWT 3Bmini.

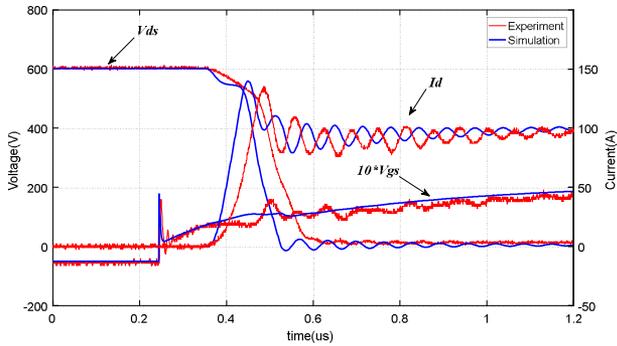


Fig. 11. Comparison of experiment and simulation turn-ON waveforms with the model of linear  $C_{gs}$  @600 V 85 A.

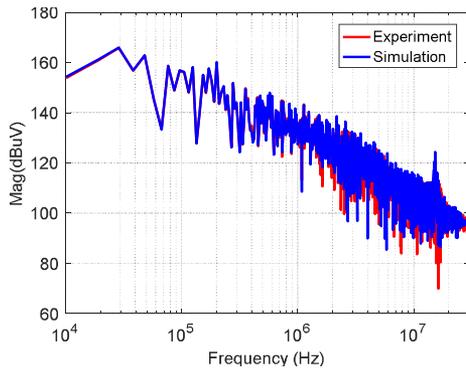


Fig. 12. Comparison of drain-source voltage spectra of experiment and simulation.

In addition, as temperature characteristics are not considered in this paper, all experiments are done at room temperature ( $\sim 25^\circ\text{C}$ ).

Circuit analysis is implemented in a commercial software, named ANSYS **Simplorer**, as shown in Fig. 7. Stray inductance of the dc loop is measured by an Agilent E4990A impedance analyzer and is added to the circuit. Gate circuit stray inductance is added to the circuit. Output voltage rise and fall time of the gate driver are considered, which can be regarded as about 10 ns.

Double pulse test results of the two models, the improved model, and the linear  $C_{gs}$  model are compared with experiment results, shown as follows. Figs. 8 and 9 compare experiment results and simulation results of the device turn-OFF waveforms. Figs. 10 and 11 compare experiment results and simulation results of the device turn-ON waveforms. The red lines represent the experiment waveforms, and the blue lines represent the simulation waveforms.

It can be seen from Figs. 8 and 10 that the improved model can correctly represent the switching transient waveforms. The drain current of the SiC MOSFET is 85 A before its turn-OFF transient, and during its turn-ON transient the peak drain current reaches about 140 A.

For previous models, which regard  $C_{gs}$  as a linear value simply, turn-OFF waveforms comparison between experiment and simulation in Fig. 9 shows little difference. However, a serious deviation occurs in turn-ON switching transient as

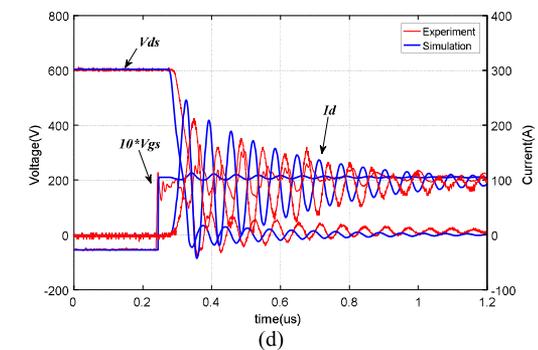
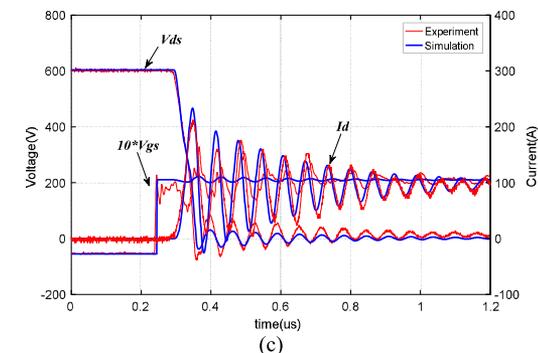
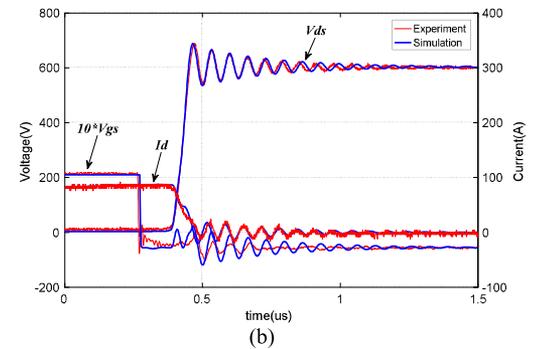
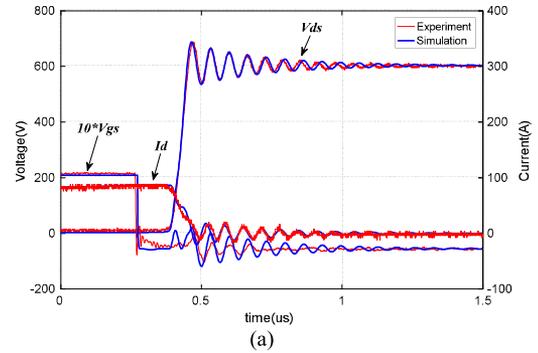


Fig. 13. Comparison of experiment and simulation waveforms when  $R_g = 0$  Ohm. (a) Turn-OFF waveforms with the improved model. (b) Turn-OFF waveforms with the model of linear  $C_{gs}$ . (c) Turn-ON waveforms with the improved model. (d) Turn-ON waveforms with the model of linear  $C_{gs}$ .

shown in Fig. 11, which can be regarded as the result of smaller  $C_{gs}$  when the drive voltage starts from negative values. The internal gate resistance  $R_g$  is measured by an LCR meter and can be considered as correct.

To do the EMI analysis, the results need to be carried out in frequency domain. The experimental drain-source voltage

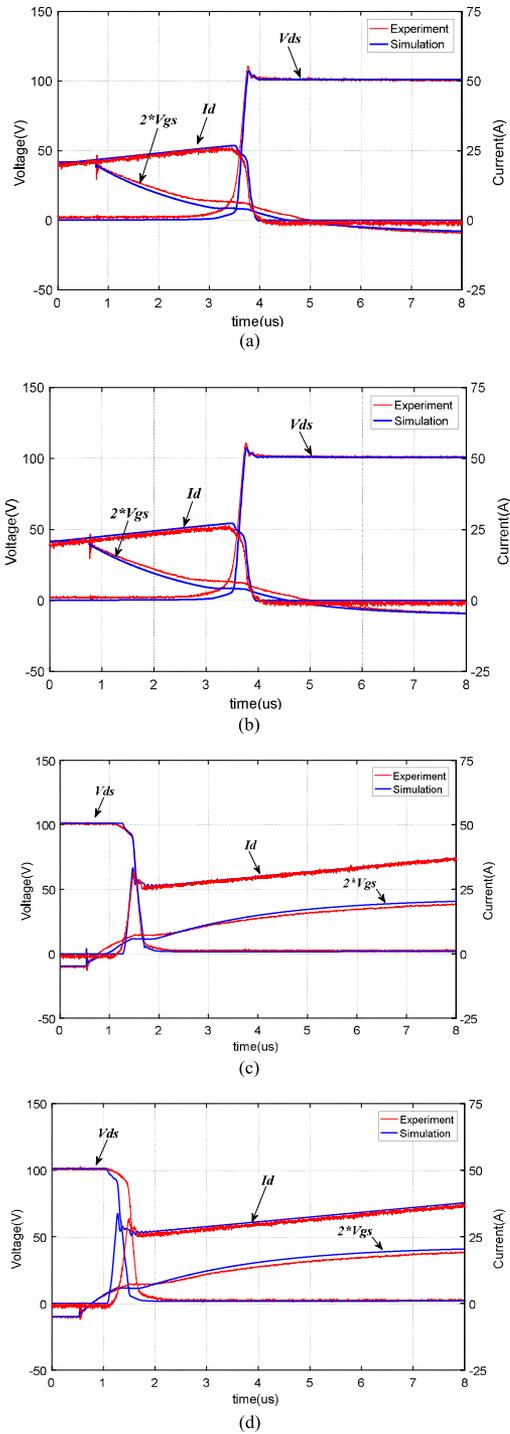


Fig. 14. Comparison of experiment and simulation waveforms when  $R_g = 67.3 \text{ Ohm}$ . (a) Turn-OFF waveforms with the improved model. (b) Turn-OFF waveforms with the model of linear  $C_{gs}$ . (c) Turn-ON waveforms with the improved model. (d) Turn-ON waveforms with the model of linear  $C_{gs}$ .

waveform and the simulated drain–source voltage waveform are synthesized for 100 cycles, and their spectra are computed by the fast Fourier transformation. Comparison of drain–source voltage spectra of experiment and simulation is plotted in Fig. 12. The red one represents the spectrum of experiment, and the blue one represents the spectrum of simulation.

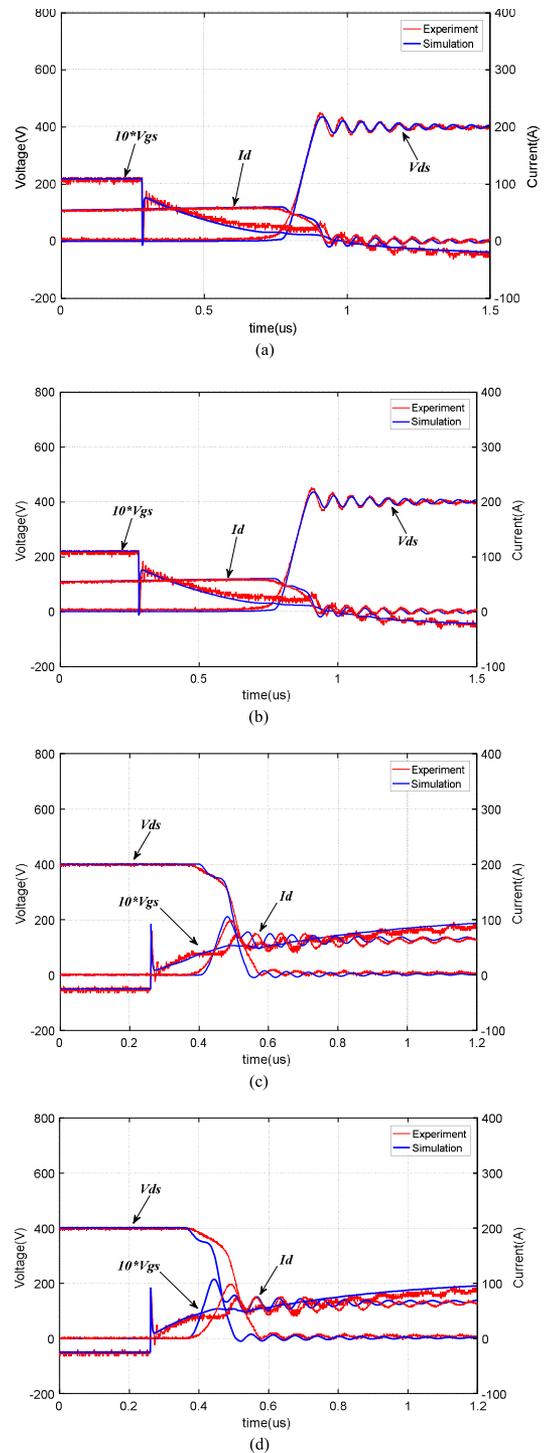


Fig. 15. Comparison of experiment and simulation waveforms when  $V_{dc} = 400 \text{ V}$ . (a) Turn-OFF waveforms with the improved model. (b) Turn-OFF waveforms with the model of linear  $C_{gs}$ . (c) Turn-ON waveforms with the improved model. (d) Turn-ON waveforms with the model of linear  $C_{gs}$ .

As shown in Fig. 12, the spectrum of simulated drain–source voltage agrees well with the spectrum of experimental drain–source voltage.

To verify the model for different external gate resistances, an external gate resistance  $0\text{-}\Omega$  is adopted while other test

TABLE II  
DYNAMIC CHARACTERISTIC PARAMETERS OF EXPERIMENTS AND SIMULATIONS

Test conditions		Experiment	Simulation with improved model	Difference compared with experiment	Simulation with model of linear $C_{gs}$	Difference compared with experiment
600 V 85 A	Turn ON	$T_{d(on)} = 0.169 \mu s$	$T_{d(on)} = 0.164 \mu s$	2.96%	$T_{d(on)} = 0.131 \mu s$	<b>22.5%</b>
		$T_r = 0.0474 \mu s$	$T_r = 0.042 \mu s$	11.4%	$T_r = 0.042 \mu s$	
		$E_{on} = 4.5666 \text{ mJ}$	$E_{on} = 4.7001 \text{ mJ}$	2.92%	$E_{on} = 4.7194 \text{ mJ}$	
	Turn OFF	$T_{d(off)} = 0.5067 \mu s$	$T_{d(off)} = 0.5105 \mu s$	0.7%	$T_{d(off)} = 0.5105 \mu s$	
		$T_f = 0.1468 \mu s$	$T_f = 0.1400 \mu s$	4.6%	$T_f = 0.1400 \mu s$	
		$E_{off} = 3.7702 \text{ mJ}$	$E_{off} = 3.9384 \text{ mJ}$	4.5%	$E_{off} = 3.9631 \text{ mJ}$	
500 V 72 A	Turn ON	$T_{d(on)} = 0.1678 \mu s$	$T_{d(on)} = 0.163 \mu s$	2.86%	$T_{d(on)} = 0.1300 \mu s$	<b>22.5%</b>
		$T_r = 0.0418 \mu s$	$T_r = 0.036 \mu s$	13.9%	$T_r = 0.037 \mu s$	
		$E_{on} = 2.9148 \text{ mJ}$	$E_{on} = 3.0004 \text{ mJ}$	2.94%	$E_{on} = 3.0123 \text{ mJ}$	
	Turn OFF	$T_{d(off)} = 0.5042 \mu s$	$T_{d(off)} = 0.5130 \mu s$	1.75%	$T_{d(off)} = 0.5130 \mu s$	
		$T_f = 0.1392 \mu s$	$T_f = 0.1230 \mu s$	11.6%	$T_f = 0.1230 \mu s$	
		$E_{off} = 2.3361 \text{ mJ}$	$E_{off} = 2.2012 \text{ mJ}$	5.77%	$E_{off} = 2.2156 \text{ mJ}$	
400 V 58 A	Turn ON	$T_{d(on)} = 0.1678 \mu s$	$T_{d(on)} = 0.1600 \mu s$	4.6%	$T_{d(on)} = 0.1300 \mu s$	<b>22.5%</b>
		$T_r = 0.0362 \mu s$	$T_r = 0.0310 \mu s$	14.4%	$T_r = 0.0330 \mu s$	
		$E_{on} = 1.7772 \text{ mJ}$	$E_{on} = 1.7748 \text{ mJ}$	1.11%	$E_{on} = 1.8207 \text{ mJ}$	
	Turn OFF	$T_{d(off)} = 0.5090 \mu s$	$T_{d(off)} = 0.5200 \mu s$	2.2%	$T_{d(off)} = 0.5200 \mu s$	
		$T_f = 0.1380 \mu s$	$T_f = 0.1220 \mu s$	11.6%	$T_f = 0.1220 \mu s$	
		$E_{off} = 1.3759 \text{ mJ}$	$E_{off} = 1.2778 \text{ mJ}$	7.13%	$E_{off} = 1.2823 \text{ mJ}$	

conditions are the same as before. Double pulse test results are shown in Fig. 13.

As shown in Fig. 13(a) and (c), switching transient waveforms of the improved model and experiment match well. For the model of linear  $C_{gs}$ , though turn-OFF waveforms comparison between experiment and simulation shows little difference [see Fig. 13(b)], a serious deviation occurs in turn-ON switching transient [see Fig. 13(d)]. This can be regarded as the result of smaller  $C_{gs}$  when the drive voltage starts from negative values.

Then, to verify the model for gate resistance higher than  $10 \Omega$ , an external gate resistance  $67.3\text{-}\Omega$  is adopted. The test dc supply voltage was 100 V. Double pulse test results are shown in Fig. 14.

As shown in Fig. 14(a) and (c), turn-OFF and turn-ON switching transient waveforms of the improved model and experiment match well. For the model of linear  $C_{gs}$ , though turn-OFF waveforms comparison between experiment and simulation shows little difference [see Fig. 14(b)], a serious deviation occurs in turn-ON switching transient [see Fig. 14(d)]. This can also be regarded as the result of smaller  $C_{gs}$  when the drive voltage starts from negative values.

To verify the model under different voltages, double pulse test results when dc voltage is 400 V while other test conditions are the same as the initial one are shown in Fig. 15.

As shown in Fig. 15(a) and (c), switching transient waveforms of the improved model and experiment match well. For the model of linear  $C_{gs}$ , though turn-OFF waveforms comparison between experiment and simulation shows little difference [see Fig. 15(b)], a serious deviation occurs in turn-ON switching transient [see Fig. 15(d)]. This can be regarded as the result of smaller  $C_{gs}$  when the drive voltage starts from negative values.

To verify the model in a further step, different dc voltages are applied to the double pulse test circuit, while other test conditions are the same as the initial one. Dynamic characteristic parameters are used as accuracy metrics of the model. They are turn-ON delay time  $t_{d(on)}$  and turn-OFF delay time  $t_{d(off)}$ , current rise time  $t_r$  and current fall time  $t_f$ , turn-ON switching

energy  $E_{on}$ , and turn-OFF switching energy  $E_{off}$ . The original experiment data are stored in csv format and postprocessed in software MATLAB. The reprocessing progress includes delay time compensation of the current probe, which is about 25 ns, and loss calculation, which is an integral operation of the voltage and current data. The test results are listed in Table II.

As shown in Table II, for the improved model, at all test points, compared with the experiment results, the switching power loss differences are less than 10%. The drain current rise time and fall time differences are less than 15%. The turn-ON and turn-OFF delay time differences are less than 5%. However, for the model which treats  $C_{gs}$  as a linear value, though other dynamic characteristic parameters are almost the same as the improved model, turn-ON delay time differences between experiment and simulation results are more than 20%. Test results prove that, compared with the model which takes  $C_{gs}$  as a linear value, the proposed improved model shows much better matching with the measured results.

Model complexity limits model usability and thus is significant for model applications. The proposed model is described by just about 7 equations and 20 parameters. These parameters can be extracted from manufacturer datasheets, simple LCR meter test, or test waveforms. The procedures of parameters extraction are simple and the consumption is low. Compared with analytical models, which uses device structural constants, the proposed model is simple. Such a model is not time consuming, and it can be well used in circuit simulations.

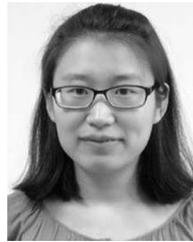
#### IV. CONCLUSION

In this paper, by a datasheet and measurement combined modeling method, an improved behavioral model of SiC power MOSFET is proposed using SPICE language. By the software Q3D, parasitic parameters of the power module are extracted and considered. Adopting the Shichman–Hodges model and extracting steady-state parameters from the datasheet, the steady-state model is obtained. The steady-state characteristics of the

model are in good accordance with those in datasheet. Then, nonlinear interelectrode junction capacitances are studied in detail. Voltage-dependent capacitances  $C_{gd}^*$  and  $C_{ds}$  are described by empirical formulas. In addition to the existing SiC MOSFET model, nonlinearity of gate–source capacitance  $C_{gs}$  because of negative gate drive voltage is considered and redefined. A continuously differentiable function is proposed to describe  $C_{gs}$ , thus convergence problems can be avoided. Simulation results are compared with the experiment results in a double pulse test circuit under different supply voltages. Comparison results show that without consideration of negative gate voltage, which impacts the gate–source capacitance, significant deviations for turn-ON delay time occur. However, simulation results of the proposed improved model show much better matching with the experiment results. Therefore, the proposed modeling method is verified. In addition, the model is simple enough and very suitable to be used in circuit simulations. The proposed model can be employed to evaluate EMI, power losses, and operation performances of SiC power MOSFET before prototype implementation, and can also be used to simulate and analyze the converter functions. In this way, cut-and-try cost and time in design approaches can be reduced.

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